BIO-DATA

1. Name : **SARAVANAN S**
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3. **EDUCATIONAL QUALIFICATION**

Degree	Specialization	Institution	Year of Graduation
M.E.	VLSI Design	Kongu Engineering College, Perundurai	June 2010
B.E.	Electronics and Communication Engineering	Adhiyamaan College of Engineering, Hosur	April 2006

4. Specialization : Low Power VLSI Design, Approximate Computing

5. Teaching Experience : 13 Years

6. **PROFESSIONAL EXPERIENCE:**

S.No.	Institution	Designation	From	To
1	K. S. R. College of Technology, Tiruchengode	Assistant professor	Dec 2013	Till date
2	Anna University Regional Centre Coimbatore	Teaching Assistant	Nov 2012	Dec 2013
3	Adhiyamaan College of Engineering, Hosur	Assistant professor	June 2010	Nov 2012

7. **PUBLICATIONS :**

1. Raghul R, Ramanitharan J, Vimalraj R and **Saravanan S**, "Design and Implementation of Approximate Truncated adder using kogge stone adder for low power applications" 2nd International Conference on Vision Towards Emerging Trends in Communication and Networking Technologies (ViTECoN) 2023, May 5 & 6 at VIT, Vellore

2. **Saravanan S** and Poovarasn R, 'FPGA Implementation of FIR Filter using Approximate Computing', Proceedings of the First International Conference on Artificial Intelligence and Machine Learning Applications, May - 2022.
3. **Saravanan S**, Deepak P, Gowrisankar V And Kavin V, 'ALU Design using Vedic Mathematics', Proceedings of the First International Conference on Artificial Intelligence and Machine Learning Applications, May - 2022.
4. Thiruvenkadam Krishnan, Parthibaraj Anguraj, **Saravanan S**, Vidya A and Sivanandam K, 'Design of Area Efficient Unified Binary/Decimal Adder/Subtractor Using Triple Carry Based Prefix Adder', Eight International Conference on Advanced Computing and Communication Systems (ICACCS), 2022.
5. **Saravanan S**, Harish T, Vasim Khan A and Hari P V, 'FPGA Implementation of Approximate Adder for Image Processing', International Research Journal of Modernization in Engineering Technology and Science (IRJMETS), Vol. 3, Issue 4, April 2021.
6. Thiruvenkadam Krishnan and **Saravanan S**, 'Design of Low-Area and High Speed Pipelined Single Precision Floating Point Multiplier', Proceedings of the Sixth International Conference on Advanced Computing and Communication Systems (ICACCS), pp. 1259-1264, 2021. DOI: 10.1109/ICACCS48705.2020.9074366.
7. Sivanandam K, Ramya R and **Saravanan S**, 'Smart travel history tracking and data management using unified mandatory card with QR code for COVID-19 in India', Proceedings of the AICTE sponsored International E-Conference on Electrical, Communication and Computing (ICECC 2020) –August 2020.
8. Thiruvenkadam Krishnan, **Saravanan S**, Parthibaraj Anguraj and Anjali S.Pillai, 'Design and implementation of area efficient EAIC modulo adder', Elsevier Materials Today: Proceedings, July 2020. Volume 33, Part 7, Pages 3751-3756. https://doi.org/10.1016/j.matpr.2020.06.172
9. Thiruvenkadam Krishnan, **Saravanan S**, Parthibaraj Anguraj and Anjali S.Pillai, 'Design of high-speed RCA based 2-D bypassing multiplier for FIR filter', Elsevier Materials Today: Proceedings, July 2020. Volume 33, Part 7, Pages 3692-3696 https://doi.org/10.1016/j.matpr.2020.05.803
10. Thiruvenkadam Krishnan and **Saravanan S**, 'Detection of Leukemia and Sickle Cell Anemia using Segmentation of Microscopic Images', Bioscience Biotechnology Research Communications, vol. 13 No.2, June 2020. http://dx.doi.org/10.21786/bbrc/13.2/77
11. Rithumika S S, Saravanan V, Venkatesh C, Sundhareshwaran N and **Saravanan S**, 'FPGA Based Hardware Trojan Detection', International Research Journal of Modernization in Engineering Technology and Science (IRJMETS), Vol. 2, Issue 4, April 2020.
12. **Saravanan S**, Jawahar K R, Lekha T, Masilsa M and Nandhini Devi K, 'Smart Pantry System Using Internet of Things', Proceedings of International Conference on Innovative Engineering Initiatives, 2019.
13. **Saravanan S**, Balachandran , Deepika, Dhayanandhi, Dhivya Priya, 'FPGA Implementation of FIR Filter Using High Speed Vedic Multiplier', International Journal of Science and Innovative Engineering and Technology, pp. 1-7,2018.

14. **Saravanan S**, Nithiyamalani V, Rajesh K, SalaiYugapathi K, Siddeshwaran V, 'FPGA Implementation of Reconfigurable Floating Point Multiplier', Proceedings of National Conference on Frontiers in Communication and Signal Processing Systems, pp. 48-56, 2017.
15. **Saravanan S**, Anitha S, Bharath R, Chiranjeevi S M, Joshi Norbert A, 'Vehicle Tracking and Fuel Monitoring System using Arduino', National Level Conference On Convergent Communication Technologies and Telemedicine Networking, pp. 44-48, 2016.
16. **Saravanan S** and Malathi D, "High Speed Multiplier Using Majority Function Based Full Adder" in proceedings of 'First international conference on Intelligent Information Systems and Management 2010(IISM 2010)' June 10-13 2010 at RVS College of Engineering and Technology, Coimbatore.
17. **Saravanan S** and Malathi D, "High Speed Multiplier Using Majority Function Based Full Adder" in proceedings of 'First international conference on Intelligent Information Systems and Management 2010(IISM 2010)' June 10-13 2010 at RVS College of Engineering and Technology, Coimbatore.

8. **List of Workshops / Seminar / STTP/FDPs Attended**

S.No	FDP/STTP/WORKSHOP	Organized By	From	To
1	Workshop on FPGA Design Using Xilinx Vivado and Mentor Graphics	K.Ramakrishnan College of Technology	14.06.2023	
2	Workshop on Breakthrough Technologies for Engineering Education and Research	NITTR Chennai	21.01.2023	
3	Design Thinking	ICT Academy at Adhiyamaan College of Engineering, Hosur	28.11.2022	29.11.2022
4	FDP on Inculcating Universal Human Values in Technical Education	AICTE	11.07.2022	15.07.2022
5	Embedded System Design Intel SoC FPGAs	SGGS Institute of Engineering and Technology, Nanded	27.01.2022	29.01.2022
6	Train the Tainer	Tessolve Semiconductor Pvt. Ltd, Bengaluru.	13.09.2021	17.09.2021

7	Machine Learning Techniques in VLSI Design	M.S.Ramaiah Institute of Technology	26.07.2021	30.07.2021
8	Machine Learning Applications in Micro-Nano VLSI Technologies	BVRIT Hyderabad College of Engineering for Women	21.06.2021	25.06.2021
9	Webinar on CAD for VLSI Design	KRCT, Trichy	23-05-2020	
10	Online FDP on "Python"	VIT, Vellore	05-05-2020	09-05-2020
11	Online Course on "Digital Circuits"	NPTEL	July, 2019	Oct, 2019
12	Online course on "Hardware Modeling Using Verilog"	NPTEL	Aug, 2018	Sep, 2018
13	FDP on "Hardware Modeling Using Verilog"	NPTEL	Aug, 2018	Sep, 2018
14	FDP on "Xilinx SoC: FPGA Based Design"	Electronics & ICT Academy, IIT Guwahati at NIT Trichy	30-07-2018	03-08-2018
15	Two Week ISTE STTP on CMOS, Mixed Signal and Radio frequency VLSI Design Conducted by IIT Kharagpur	K.S.Rangasamy College of Technology, Tiruchengode	30-01-2017	04-02- 2017
16	Faculty Development Programme on Learning Improvement Techniques	PALS, IIT Madras	09-11-2016	11-11-2016
17	Faculty Empowerment workshop on VLSI Design & Laboratory	EQIP Foundation at K.S.Rangasamy College of Technology, Tiruchengode	09-12-2014	13-12-2014
18	Faculty Development Training Programme on Digital Communication	Sri Ramakrishna Engineering College Coimbatore	10.06.2013	16.06.2013
19	Mentor Graphics Based VLSI Design Flow	Anna University Coimbatore	24.04.2010	
20	Workshop on "VLSI Testing and Circuit Edit"	Tessolve Semiconductor Pvt Ltd, Bangalore.	21.07.2009	23.07.2009